What is claimed is:

1. A method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification of the circuit design, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. manually modifying the analysis if verification of the circuit design over the analysis region results in false;

repeating steps b-c until the circuit design is verified; and

repeating steps b-c until a user identifies an error in the circuit design.

2. The method according to claim 1, wherein the step of manually modifying the analysis comprises the steps of:

a. selecting a signal in the analysis region; and

b. adding a portion of the circuit design relating to the signal in the analysis region.

3. The method according to claim 2, wherein the step of selecting the signal in the analysis region is performed by selecting the signal from a Plot window.

4. The method according to claim 2, wherein the step of selecting the signal in the analysis region is performed by selecting the signal from a Source Code window.

5. The method according to claim 2, wherein the step of adding a portion of the circuit design relating to the signal in the analysis region comprises adding the articulated fan-in driving the signal to the analysis region.

6. The method according to claim 5, wherein the step of adding the articulated fan-in driving the signal to the analysis region comprises identifying the articulated fan-in of the signal by traversing the circuit design backwards from the signal until a signal

from the group of: primary inputs, storage elements and articulation points is encountered.

7. The method according to claim 2, wherein the step of adding a portion of the circuit design relating to the signal in the analysis region comprises adding a portion of the articulated fan-in driving the signal to the analysis region.

8. The method according to claim 7, wherein the step of adding a portion of the articulated fan-in driving the signal to the analysis region comprises adding a portion of the articulated fan-in driving the selected signal that is 'turned on' by current value assignments in the Plot window to the analysis region.

9. The method according to claim 1, wherein the step of manually modifying the analysis comprises the steps of:

   a. selecting a signal in the Plot window at time cycle just after the circuit design is reset; and

   b. adding the reset portion of the articulated fan-in of the selected signal in the analysis region.

10. The method according to claim 1, wherein the step of manually modifying the analysis comprises the steps of:

   a. selecting a signal in a Plot window at a time cycle other than just after the circuit design is reset; and

   b. adding a non-reset portion of the articulated fan-in of the selected signal in the analysis region.

11. The method according to claim 1, wherein the step of manually modifying the analysis comprises the steps of:

   a. the user selecting an articulation point inside the analysis region; and

   b. removing the articulated fan-in of the articulation point from the analysis region;

12. The method according to claim 1, wherein the step of manually modifying the analysis comprises the steps of:

a. the user selecting an articulation point at the boundary of the analysis region; and

b. adding the articulated fan-in driving the selected articulation point to the analysis region.

13. The method according to claim 1, wherein manually modifying the analysis comprises the steps of:

a. the user selecting at least one signal in the analysis region from the Plot window, wherein each signal is selected at a specific time cycle;

b. generating a triple based on each selected signal, wherein a triple comprises the name of the selected signal, the specific time cycle of selection and the value of the selected signal at the specific time cycle;

c. generating a rule based on the triples;

d. verifying the rule separately; and

e. verifying the circuit design using the rule as an assumption for the analysis region.

14. The method according to claim 13, wherein the rule is automatically modified in case the step of verifying of the rule results in non-verification.

15. A method for guiding formal verification for a circuit design in circuit simulation software to optimize time required for verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false;

d. automatically modifying the analysis region using the candidate signals; and

e. manually modifying the analysis region if there are no appropriate candidate signals;

repeating steps b-e until the circuit design is verified; and

repeating steps b-e until a user identifies an error in the circuit design.

16. The method according to claim 15, wherein the step of identifying the candidate signals for modification of the analysis region if verification of the circuit design is false comprises identifying articulation points corresponding to the analysis region as the candidate signals.

17. The method according to claim 16, wherein the step of automatically identifying articulation points corresponding to the analysis region comprises the steps of:

a. identifying comparison statements on wide signals as articulation points; and

b. identifying Boolean guards of conditional statements as articulation points.

18. The method according to claim 15, wherein the step of automatically modifying the analysis region using the candidate signals include prioritizing the candidate signals on the basis of productivity choices.

19. The method according to claim 18, wherein the step of prioritizing candidate signals on the basis of productivity choices comprises the steps of:

a. assigning productivity weights to analysis region modification choices;

b. ranking the choices according to the productivity weights wherein the choices with positive productivity weights are considered as high-productivity choices and the choices with negative weights are considered low-productivity choices; and

c. identifying the highest-productivity choices from the high-productivity choices.

20. The method according to claim 15, wherein the step of automatically modifying the analysis region comprises expanding the analysis region by including the articulated fan-in corresponding to the highest-productivity choices that are located at the boundary of the analysis region.

21. The method according to claim 15, wherein the step of automatically modifying the analysis region comprises removing the articulated fan-in corresponding to the highest-productivity choices that are located inside the analysis region from the analysis region.

22. The method according to claim 18, wherein the step of automatically modifying the analysis region comprises modifying the analysis region using low-productivity choices on the user's decision in case there are no high-productivity choices.

23. The method according to claim 15, wherein the step of manually modifying analysis if there are no appropriate candidate signals, comprises the steps of:

a. defining an abstraction created in response to the low productivity choices in the analysis region;

b. proving the abstraction in the circuit design separately; and

c. verifying the circuit design using the abstraction in the analysis region.

24. The method according to claim 23, wherein the step of defining an abstraction comprises adding new logic to the circuit design corresponding to the abstraction.

25. The method according to claim 15, wherein the step of manually modifying the analysis if there are no appropriate candidate signals, comprises the steps of:

a. defining an assumption created in response to low productivity choices in the analysis region;

b. proving the assumption in the circuit design separately; and

c. verifying the circuit design using the assumption in the analysis region.

26. The method according to claim 15, wherein the step of manually modifying the analysis includes the steps of:

a. the user selecting at least one signal in the analysis region from a Plot window, wherein each signal is selected at a specific time cycle;

b. generating a triple based on each selected signals, wherein a triple comprises the name of the selected signal, specific time cycle of selection and the value of the selected signal at the specific time cycle;

c. generating a rule based on the triples;

d. verifying the rule separately; and

e. verifying the circuit design using the rule as an assumption for the analysis region.

27. The method according to claim 26, wherein the rule is automatically modified in case the step of verifying of the rule results in a false.

28. The method according to claim 15, wherein the step of manually verifying the circuit design by applying formal verification over the analysis region comprises user deciding that there is an error in the circuit design in case there are no high-productivity choices.

29. A method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for the verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying articulation points corresponding to the analysis region as analysis region modification choices;

d. automatically modifying the analysis region using the articulated fan-in of the analysis region modification choices if verification of the digital design over the analysis region results in a false;

repeating steps b-d until the circuit design is verified; and

repeating steps b-d until a user identifies an error in the circuit design.

30. A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules;

31. The system according to claim 30, wherein the system for guiding formal verification of a circuit design to optimize time required for verification process further comprises a Productivity Choice Determination tool to determine high-productivity choices for expanding the analysis region if verification fails.

32. The system according to claim 30, wherein the system for guiding formal verification of a circuit design to optimize the time required for verification process further comprises an Articulation Point Selection tool to identify articulation points corresponding to the analysis region to choose smaller analysis region for circuit verification.

33. The system according to claim 30, wherein the system for guiding formal verification of a circuit design to optimize time required for verification process further comprises a Rule Verifier for verifying user defined rules for the analysis region.

34. The system according to claim 30, wherein the system for guiding formal verification of a circuit design to optimize time required for verification process further comprises a database for storing a set of triples based on a set of signals selected by the user.

35. The system according to claim 30, wherein the GUI comprises a Source Code window for enabling the user to select a signal from a source code displayed.

36. The system according to claim 30, wherein the GUI comprises a Plot window for enabling the user to select a signal at a specific time cycle from the waveform of the signal displayed to the user.

37. A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules;

d. a Productivity Choice Determination tool to determine high-productivity choices for expanding the analysis region if verification fails;

e. an Articulation Point Selection tool to identify the articulation points corresponding to the analysis region to choose smaller analysis region for circuit verification;

f. a Rule Verifier for verifying user defined rules for the analysis region; and

g. a database for storing a set of triples based on a set of signals selected by the user.

38. A method as recited in claim 1, wherein the method is implemented as a computer program product.

39. A method as recited in claim 15, wherein the method is implemented as a computer program product.

40. A method as recited in claim 29, wherein the method is implemented as a computer program product.